1.0 Features

- **320 X 256 Pixels**
- **Snapshot Mode**
- **P on N Input Polarity**
- **18 Million Electron Well Capacity**
- **Flexible Integration Control**
  - **Integrate-While-Read**
  - **Integrate-Then-Read**
- **Selectable, 1 to 4 Outputs**
- **Dynamic Image Transposition**
  - **Image Invert [top-to-bottom]**
  - **Image Revert [left-to-right]**
- **Dynamic Windowing Readout**
- **Selectable Differential Output Mode**
- **On-Chip DACs control**
  - **Detector Bias**
  - **Power Adjust**
- **Variable Gain**
- **Signal 'Skimming'**
- **Buffered Temperature Sensor Output**
- **High-Voltage QWIP Bias Compatibility**
- **Adjustable Power**
  - **Low Power Operation**
  - **High Speed Operation**
- **Two Operational Modes**
  - **Simple 'hands-off' Default Mode**
  - **User Configurable Command Mode**
- **Tested Wafer w/ Wafer Map and Die Data.**
- **Detector Applications**
  - **InSb, InGaAs, MCT, or QWIP**

2.0 Product Description

The ISC9705 is a high performance, 320 x 256 pixel, readout integrated circuit (ROIC) with snapshot mode integration. This state-of-the-art ROIC is suitable for use with p on n detector materials such as indium antimonide (InSb), mercury cadnium telluride (MCT), quantum well infrared photo diodes (QWIPs) and indium gallium arsendide (InGaAs). A simplified 'hands-off' Default Mode directly supports single output NTSC or PAL operation. Using the Command Mode, the ISC9705 supports advanced features including; dynamic image transposition, dynamic windowing, multiple output configurations, and signal 'skimming'. Both modes support integrate-while-read and integrate-then-read operations, variable gain, biasing techniques for high and low reverse bias detectors and signal "skimming".

Using four outputs, frame rates up to 346 frames per second can be achieved for full 320 x 256 frames. Using the dynamic windowing mode, small windows can be read out at up to 15,600 frames per second. A convenient buffered temperature sensor output is available for monitoring of the ROIC substrate temperature.

The ISC9705 is fabricated using an advanced 0.6 micron single poly, double metal process which utilizes high speed CMOS transistors. High speed, precision analog circuits are combined with high density digital logic circuits. The ISC9705 is delivered in wafer form and is specified for operation from 80 K to 300 K.

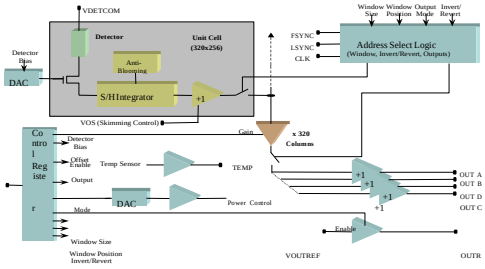


Figure 1. ISC9705 Block Diagram

Figure 1 shows the block diagram for the Default Mode operation. The detector bias generator is adjustable using the VDET_ADJ pad. The unit cell uses a direct injection topology with an anti-blooming transistor. The output from each unit cell is then addressed to a column bus and sampled onto a variable gain column amplifier. The column amplifier is multiplexed to a single output. A skimming function is also provided to globally offset the output signal for high leakage current detectors such as QWIPs. An on-chip temperature sensor is available through the TEMP pad. Power control is accomplished by applying a voltage to the IMSTR_ADJ pad. The ISC9705 pad definition is shown in Figure 2. The pads required for both operation modes appear in bold type.

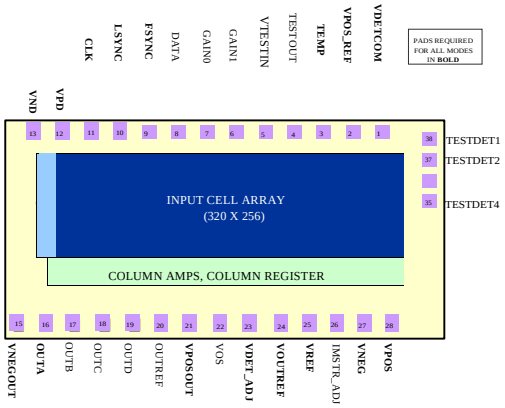


Figure 2. ISC9705 Pinout

3.1 Specifications

Maximum Ratings					
Parameter	**With Respect To**	**Min.**	**Max.**	**Absolute Max.**	**Units**
VPOS,VPD,VPOSOUT	VNEG,VND,VNEGOUT,Vsub	-0.5	5.5	6.0	Volts
Vref	VNEG,VND,VNEGOUT,Vsub	-0.5	VPOS		Volts
Clock Inputs	VNEG,VND,VNEGOUT,Vsub	-0.5	VPD + 0.2		Volts

NOTES:
Stresses above the values listed may cause permanent damage to the device. Exposure to absolute maximum ratings for even short periods of time may cause permanent damage to the device.

Temperature Ranges			
Parameter	**Min.**	**Max.**	**Units**
Operating[1]	50	300	K
Storage[2]	50	400	K

NOTES:
1. The operating temperature range is the range over which the device will meet specifications.
2. Exposure to temperatures beyond the storage range can result in permanent damage to the device. Devices should be stored in a dry box over an extended period of time.

Mechanical Specifications					
Parameter	**Test Level**	**Min.**	**Typ.**	**Max.**	**Units**
Wafer Size	V		5		Inch
Total Die per Wafer [1]	V		72		Die/wafer
Detector Columns	IV		320		Active unit cells
Detector Rows	IV		256		Active unit cells
Detector Row and Column Pitch	IV		30		µm
Die Size [2]	IV		11.35 x 10.65		mm
Scribe Lanes in X and Y	IV		200		µm

NOTES:
1. Including all die grades
2. As measured to edge of scribe lane

EXPLANATION OF TEST LEVELS
Test Level
I – 100% production tested.
II – 100% production tested at room temperature.
III – Sample tested only.
IV – Parameter is guaranteed by design and/or characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at room temperature.

DC Specifications (50-300K operation unless noted)					
Parameter	**Test Level**	**Min.**	**Typ.**	**Max.**	**Units**
Output Rate 300K [6]	II			6.142	Mpixels
Output Rate 80 K [6]	IV			10	MPixels
Max Full Window Frame Rate @80K (300K)					
4 Output Mode	Note 13			346(250)	Frames/sec
2 Output Mode	Note 13			202(140)	Frames/sec
1 Output Mode	Note 13			110(70)	Frames/sec
Max Frame Rate @ 80K (300K)					
4 Output Mode	IV			15.6(12)	KFPS
2 Output Mode	IV			15.6(11.5)	KFPS
1 Output Mode	IV			15.6(11.2)	KFPS
Output Voltage Swing [6]	VI	2.7	3	3.2	Volts
Output Voltage Low [6]	V		1.6		Volts
Output Voltage High [6]	V		4.6		Volts
Input Clock Rate	IV	DC	3	5 [15]	MHz
Output Noise [8]					
Gain 00	IV		130	250	µV
Gain 01	IV		155	300	µV
Gain 10	IV		200	350	µV
Gain 11	IV		340	400	µV
Equiv. Integration Capacitor Noise [8]					
Gain 00	IV		870		e^-
Gain 01	IV		760		e^-
Gain 10	IV		670		e^-
Gain 11	IV		575		e^-
Gain					
Gain 00 (Relative Gain 1.0)	IV	0.19	0.17		$\mu V/e^-$
Gain 01 (Relative Gain 1.33)	IV	0.25	0.22		$\mu V/e^-$
Gain 10 (Relative Gain 2.0)	IV	0.38	0.33		$\mu V/e^-$
Gain 11 (Relative Gain 4.0)	IV	0.65	0.60		$\mu V/e^-$
Transimpedance Non-Linearity [10]	IV		0.1%	0.5%	
Unit Cell Input					
Capacitance [7]	IV	0.1	0.3	0.5	pf
Impedance [7]	IV	1e+03	5e+04	1e+06	$Ohms*cm^2$
Full Well Capacity [11]	IV		$18e^6$	$16e^6$	e^-
Input Current [7]	IV	.020	1.0	10	nA

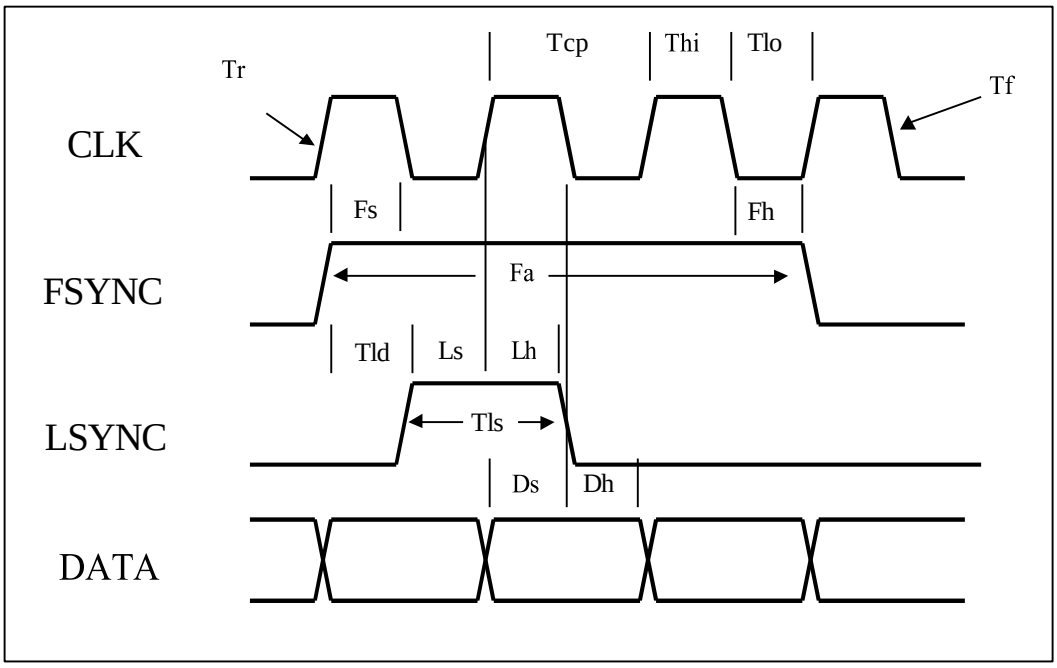
NOTES:
1. Category IV for specified min., category VI for specified max.
2. Category IV for specified min. and max., category VI for specified typ.
3. Voltages below Vnd may cause excess power dissipation.
4. Voltages above Vpd may cause excess power dissipation.
5. Typical value tested
6. 25 pf max., 100K ohms min.
7. Simulation range.
8. Zero detector current.
9. Imstr_adj set for 100 uA
10. As measured by output voltage vs Tint; Max deviation from a least squares fit over 10% to 80% full well.
11. Specified at gain 00.
12. Relative gain measured.
13. Category IV for 80K, category VI 300K
14. For high reverse bias configurations (e.g. QWIP)
15. Output pixel rate is twice the input clock rate

DC Specifications (cont)	**Test Level**	**Min.**	**Typical**	**Max.**	**Units**
On Chip Detector Bias DAC Input					
Voltage Range	VI	-100 to 400	-100 to 510	-100 to 650	mV
High Voltage Configuration	VI		800		mV
Low Voltage Configuration	VI		200		mV
DAC Bits	V		7		
Voltage Resolution	VI	3.93	4.8	5.9	mV/count
Temperature Sensor Output @ 300K	V	0.63	0.70	0.78	Volts
Temperture Sensor Output @ 77K	IV	1.00	1.10	1.20	Volts
Power Supply Voltages (wrt VNEG,VND,VNEGOUT,Vsub)					
VDETCOM	Note 1	0	5.5	8.5 [14]	Volts
VPOS	Note 1	5.3	5.5	5.7	Volts
VPOSOUT	Note 1	5.3	5.5	5.7	Volts
VPD	Note 1	5.3	5.5	5.7	Volts
Reference and Control Voltage Inputs					
VREF	Note 2	1.5	1.6	1.7	Volts
VOUTREF	Note 2	1.5	1.6	1.7	Volts
VDET_ADJ		0		5.5	Volts
IMSTR_ADJ	IV	0	3	5.0	Volts
VOS	IV	VREF		VPOS	Volts
Power Suppy Currents					
VDETCOM	V		<1	<1	mA
VPOS	V		1.6	10	mA
VPOSOUT	V		1.4	15	mA
VPD	V		0.7	1	mA
Logic Inputs					
Input Low Voltage	II	VND - 0.2 [3]	VND	VND + 0.2	Volts
Input High Voltage	II	VPD - 0.2	VPD	VPD + 0.2 [4]	Volts
Power Consumption [9]					
Single Output NTSC/PAL	IV		30		mW
Four Output Max Frame Rate	IV		120		mW
Integration Time	IV	5.1 @10MHz	User adjustable	Tframe - Treset	µsec

Switching Specifications Full Temperature Range					
Parameter	**Name**	**Min.**	**Typ.**	**Max.**	**Units**
Trise	Tr			10 [1]	ns
Tfall	Tf			10 [1]	ns
Clock Duty Cycle	Tcp	200			ns
Clock High	Thi	(Tcp / 2)* 0.98		(Tcp / 2)* 1.02	ns
Clock Low	Tlo	(Tcp / 2)* 0.98		(Tcp / 2)* 1.02	ns
FSYNC to CLK falling edge setup	Fs	15			ns
FSYNC to CLK falling edge hold	Fh	15			ns
FSYNC minimum high	Fa	11.8			µsec
FSYNC to LSYNC delay	Tld	Tcp/2			
LSYNC to CLK rising edge setup	Ls	15			ns
LSYNC to CLK rising edge hold	Lh	15			ns
LSYNC minimum high	La	1	1	1	clocks
DATA to CLK falling edge setup	Ds	15			ns
DATA to CLK falling edge hold	Dh	15			ns

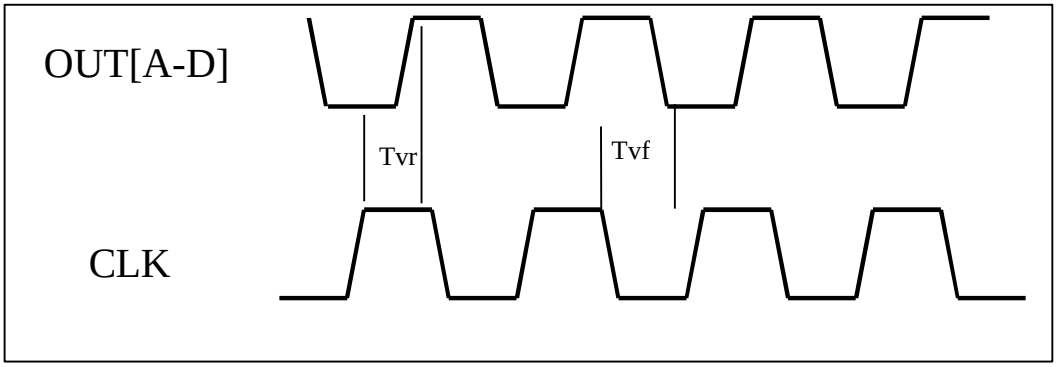
NOTES:

1. Max rise and fall times specified as the smaller of Tcp * .05 or 80ns



AC Specifications Full Temperature Range					
Parameter	**Name**	**Min.**	**Typ.**	**Max.**	**Units**
Clock rise to video output settled delay [1]	Tvr		60	80	ns
Clock fall to video output settled delay [1]	Tvf		60	80	ns
Crosstalk	Xt		0.1%	0.3%	

Notes:
1. Video data appears on both the rising and falling edges of the clock, data settling to 0.1%



4.0 Pinout Descriptions

		DIGITAL PINS	
Chip Pin	**Signal Name**	**Description**	**I/O type**
6 7	**GAIN1** **GAIN 0**	**Exteranl Gain:** These pins are used to control the gain of the chip when operating in Default Mode, they are not used in Command Mode. There are internal pull down resistors on each pin. See the DC Specification for the relative gain settings.	DI
8	**DATA**	**Serial Control Register Data**: This digital input is used to program the Serial Control Register when operating the chip in Command Mode. This input is not connected in Default Mode and is internally pulled down.	CI
9	**FSYNC**	**Frame Sync:** This signal is used to sync the start of a frame, invoke new commands loaded in the Serial Control Register and control the integration time. Frames are synced and Serial Control Register words are loaded on the rising edge of FSYNC. Integration time is started on the falling edge of FSYNC.	CI
10	**LSYNC**	**Line Sync:** This signal controls the readout synchronization of each individual row on the array. A sequence of LSYNC pulses produce a readout sequence. The rising edge of LSYNC is synchronous with the falling edge of CLK.	CI
11	**CLK**	**Data Output and Command Data Stream Clock:** This signal is used to load commands on the DATA input pin into the Serial Control Register and to read out pixel data on OUTA-D. Pixel data is clocked on both the rising and falling edge of CLK. Data is loaded into the Serial Control Register only on the falling edge of CLK.	CI

Explanation of I/O Type Symbols:
AO - Analog Output: Low bandwidth analog output.
DI - Digital Input: Low speed digital signal.
CI - Clock Input: High speed digital signal.
CO - Clock Output: High speed digital output.
P - Power Supply: Power supply or power supply return [ground].
R - Reference Voltage: DC voltage reference
TA - Test Analog Input: DC test voltage
TD - Test Detector I/O: Test detector access [used to test detectors after hybridization]
VO - Video Output: High speed video output pin.

		Analog Pins	
Chip Pin	**Signal Name**	**Description**	**I/O Type**
16	**OUTA**	**Video Output A:** Chip output pin, used for both Default and Command Mode operation in 1, 2, and 4 output modes.	VO
17	**OUTB**	**Video Output B:** Chip output pin for the for Command Mode operation in 2 and 4 output modes.	VO
18	**OUTC**	**Video Output C:** Chip output pin for the for Command Mode operation in 4 output.	VO
19	**OUTD**	**Video Output D:** Chip output pin for the for Command Mode operation in 4 output mode.	VO
20	**OUTREF**	**Common Mode Reference Output:** This pin provides a buffered version of Voutref for systems which use common mode noise reduction techniques. This output is the Voutref signal routed through a buffer amplifier identical to those used for the video output signals, used in Command Mode only	VO
3	**TEMP**	**Buffered Temperature Diode:** This pin may be used to read the temperature of the chip.	AO
24	**VOUTREF**	**Analog Output Reference Voltage:** 1.6 volts, care should be taken to prevent Voutref and Vref from AC coupling.	R
22	**VOS**	**Skimming Voltage:** Provides a means of subtracting a constant voltage from the detector signals prior to the column amplifier stage. In Command Mode it is enabled/disabled through the Serial Control Register.	R
25	**VREF**	**Analog Reference Voltage:** 1.6 volts, care should be taken to prevent Voutref and Vref from AC coupling.	R
23	**VDET_ADJ**	**Detector Bias Adjustment:** This pin provides a means to set the detector bias voltage in Default Mode. The voltage set at this pin depends on the type of detectors, detector processing and operating temperature. In Command Mode, the Serial Control Register is used to adjust detector bias and this pad can be used to monitor the setting.	R
26	**IMSTR_ADJ**	**Master Current Adjustment:** This pin provides a means to adjust the master current source level in Default Mode. In Command Mode the master current is adjusted through the Serial Control Register and this pad is not connected.	R

Power Supply and Ground Pins			
Chip Pin	**Signal Name**	**Description**	**I/O Type**
1	**VDETCOM**	**Detector Common:** Detector Postive Supply, connected to the "detector common hybridization ring. This is a ring of 6 connection pionts that surrounds the active detector area.	P
2	**VPOS_REF**	**Low Voltage Detector VDETCOM Supply:** This pin is used to power VDETCOM for low reverse bias detectors. It must be tied to the VDETCOM pad, by the user.	P
28	**VPOS**	**Analog Supply:** This is the positive supply for all analog circuits on the chip except the output multiplexer and buffer circuits.	P
12	**VPD**	**Digital Supply:** This is the positive supply for all the digital circuits.	P
21	**VPOSOUT**	**Output Supply:** This is the positive supply for the output multiplexer and buffer circuits that drive OUTA-D and OUTR. This supply is the largest AC current carrying node on the chip. Care should be taked to provide a low ESR capacitor path for this node, bypassed to VNEGOUT. Other positive supplies should be isolated from the relatively large AC currents carried by this pad.	P
13	**VND**	**Digital Return:** Ground node for all the digital circuits on the chip.	P
15	**VNEGOUT**	**Output Ground:** This ground node sinks the output amplifiers that drive the output multiplexer, OUTA-D and OUTR. This is the largest current carrying ground node on the chip and care should be taked to provide a low ESR capacitor path for this node.	P
27	**VNEG**	**Analog Ground:** Ground for all the analog circuits except the output multiplexer and buffers. This node is connected to the substrate (Vsub). Care should be taken to minimize inductance to this pad.	P

Special Use Pins			
Chip Pin	**Signal Name**	**Description**	**I/O Type**
5	**VTESTIN**	**Test Row Input Voltage:** This pad may be used to set a voltage for the test row in the chip.	TA
35, 36, 37, 38	**TESTDET (4-1)**	**Test Detector Pads:** These 4 pads provide a means of connecting to the 4 test detectors. The position of the test detectors is outlined in the Mechanical Drawing, 101-9705-80.	TD
4, 14, 29-34		**DO NOT CONNECT TO THESE PADS !** Bonding to these pads could permanently damage the performance of the chip. These pads are used for ROIC factory testing only.	

5.0 Theory of Operation

A general description of the ISC9705 operation is given in this section.

Input Circuit

The Standard 320 uses a direct injection input circuit as shown in Figure 3. Detector current flows through the input gate transistor and charges up the integration capacitor. The anti bloom gate keeps the input circuit from saturating. The voltage on the integration capacitor is sampled and multiplexed to the column amplifier. The detector bias voltage may be controlled by applying a bias on the Vdet_adj pad when in Default mode. The detector bias is also adjustable using the Serial Control Register when operating the device in Command Mode. Adjusting the detector bias this way provides approximately 4-5 mV per count. The approximate relationship between the Vdet_adj input and the detector bias is shown in Figure 4.

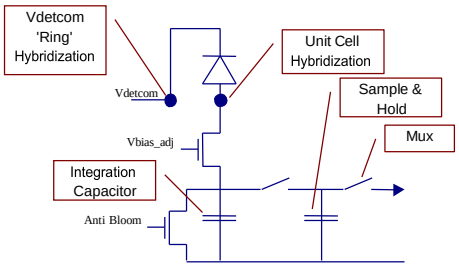


Figure 3. Simplified Unit Cell Schematic

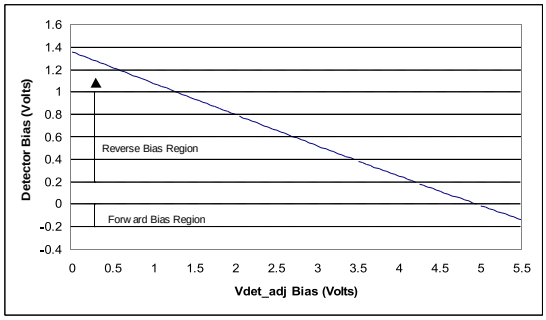


Figure 4. Detector Bias vs. Vdet_adj voltage

Column Amplifier

The column amplifier, shown in Figure 5, provides sample/hold, amplification, and skimming functions. The signal from the unit cell is sampled and held onto the column amplifier. The amplifier gain is controlled by the Gain0 and Gain1 pins when in Default Mode or by providing gain data to the Serial Control Register when in Command Mode. The relative gain is adjustable from 1 to approximately 4. A global offset function (also known as skimming) is implemented with the column amplifier and is available in both operation modes. To operate skimming, the Vos pad is set to a voltage greater than the voltage on Vref pad. The Vos voltage range is from Vref to Vpos, which corresponds to offsetting from 0 to 100% of full well. The column amplifier is also used to drive the output multiplexer bus.

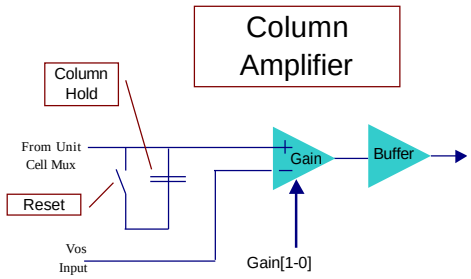


Figure 5. Column Amplifier Block Diagram

Output Multiplexer and Buffers

The ISC9705 may be run using from one to four outputs. A reference output can also be enabled. Routing of a given column amplifier to a given output buffer is accomplished through the output multiplexer, shown in Figure 6. The maximum output data rate supported in the Default Mode is 6.14MHz. In the Command Mode, output data rate up to 10MHz per output can be attained. For single output mode, all pixels are readout through OutA. When using multiple outputs, pixels are assigned to a specific output channel, and will be read out through only that channel, regardless of the invert/revert, windowing, and/or line repeat modes selected.

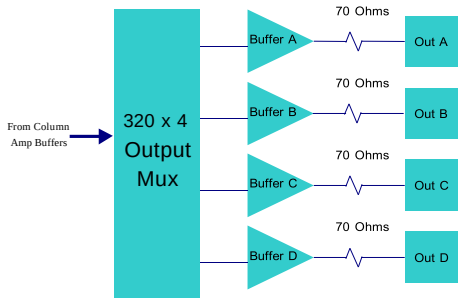


Figure 6. Output Multiplexer and Buffers

Integration Modes

The Standard 320 device features snapshot mode integration, where all pixels integrate simultaneously. The integration process is controlled by the FSYNC clock, and allows both Integrate-While-Read and Integrate-Then-Read modes of operation.

A timing pattern for the Integrated-While-Read operation is shown in the Figure 7. The rising edge of the FSYNC clock pulse marks the beginning of the frame time. This is followed by a series of LSYNC (LSYNC controls the synchronization of the readout of each individual line) pulses that produce the readout sequence. In this case, the frame time is approximately equal to the pixel readout time. The integration time occurs during the readout time, allowing for the greatest possible frame rate and integration time duty cycle (where integration time duty cycle = T_{Int} / T_{Frame}) for a given window size.

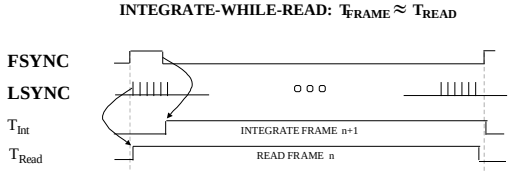


Figure 7. Integrate-While-Read timing diagram

Figure 8 shows a timing pattern for operation of the Standard 320 device in the Integrate-Then-Read mode. The rising edge of the FSYNC clock pulse marks the beginning of the frame time. This is followed immediately by a sequence of LSYNC pulses that produce a readout sequence. Note that in this case the FSYNC clock remains high until the readout sequence has been completed. The integration time occurs after the readout time, resulting in a frame time that is approximately equal to the readout time plus the integration time. This results in a lower maximum frame rate and integration time duty cycle for a given window size.

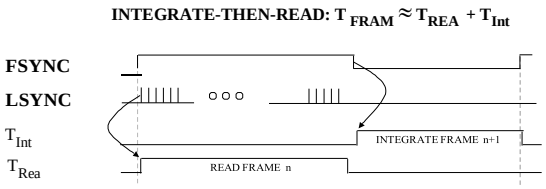


Figure 8. Integrate-Then-Read timing diagram

Biasing the Detector

It is important to bond the ISC9705 based upon the specific bias requirements for the type of detector being hybridized. There are two pads on the ISC9705 which define the detector bias interface. The first of these, the VDETCOM pad, is connected to a ring of detector common bumps that surround the active detectors. The Mechanical Interface Database (Doc # 101-9705-61) and application note "How to Interpret and Use the Mechanical Interface Database for the ISC9705" (Doc # 400-9705-21), provide additional information on this structure. The voltage applied to the VDETCOM pad sets the bias for detector common. A voltage of 0 to 8.5 volts referenced to VNEG (at 0 volts) may be supplied to this pad. The second interface pad is the VPOS_REF pad. The internal detector bias generation circuitry is referenced to VPOS_REF. The ISC9705 output signal VPOS_REF (~5.5V) provides the IC's internal reference point for the detector bias generation circuit. Any externally supplied bias generator must be referenced to VPOS_REF and not GND.

Two modes of supplying bias to the detectors are supported. For high detector bias applications (QWIP, PIN) it is advisable to reference a system supplied VDETCOM bias generator to the ISC9705 VPOS_REF pad signal. This does not imply applying a bias to VPOS_REF. For low reverse bias voltage detectors (InSb, HgCdTe), the VDETCOM pad and VPOS_REF pad are connected together by the end user.

Do not apply any bias to the VPOS_REF pad. The VPOS_REF pad is a low impedance voltage output pad from the ISC9705 to the system. Applying a bias to this pad may permanently damage the ISC9705 device.

6.1 Modes of Operation

The ISC9705 has two operation modes, the simplified Default Mode and the programmable Command Mode which utilizes the advanced features of the ROIC.

Default Mode

This mode provides a simple interface, with reduced external electronics and power dissipation, for applications where advanced ROIC features or high-speed performance are not required. The Default Mode does not use the on chip Serial Control Register. Therefore, advanced features such as windowing, invert/revert and multiple data outputs are not available. The Default Mode supports operation with both high and low reverse bias detectors by using a special biasing procedure. In Default Mode the ISC9705 operates with the following configuration:

- single output
- variable gain
- full window
- normal scan order
- no reference output
- supporting NTSC or PAL video timing
- maximum output rate 6.14MHz
- skimming

A total of 19 interconnects are required for Default Mode as shown in Figure 9.

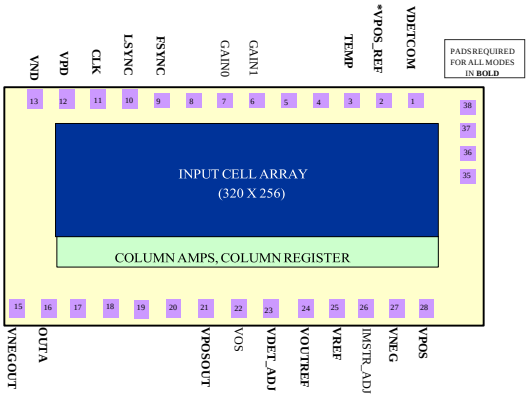


Figure 9. Default Mode Bond Pad Diagram

Command Mode

Command Mode operation utilizes the on chip Serial Control Register to control device modes and advanced readout features. The fields of the Serial Control Register are illustrated in Figure 10. To operate in this mode, the DATA pad must be used to load control words into the Serial Control Register. The settings in this register determine the gain state, detector bias setting, power bias control, master current bias, skimming setting, output mode, window size, window position, image transposition and test mode. Master clock frequencies up to 5 MHz (10 MHz output rate) are supported when operating in the Command Mode.

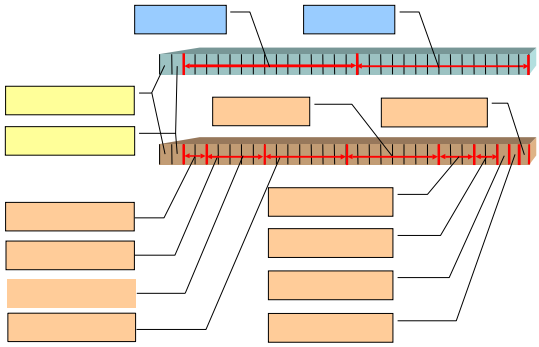


Figure 10. Serial Control Register Fields

There are 16-20 interconnects required, depending on the number of outputs and options invoked. The Command Mode bond pad diagram is shown in Figure 11.

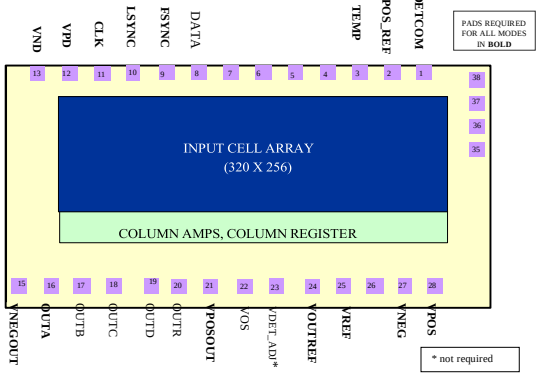


Figure 11. Command Mode Bond Pad Diagram

Output Modes

The ISC9705 can be configured to support one, two, four outputs with or without an output reference. In order to invoke any output mode other than single output, with no reference output, the device must be operated in Command Mode. For single output mode, all pixels are read out through OutA. When using multiple outputs, pixels are assigned to a specific output channel, and will be read out through only that channel, regardless of the image transposition (invert/revert), and windowing modes selected.

The lowest left-hand pixel is defined as pixel (0,0), where this annotation signifies the pixel at location row 0, column 0 of the ISC9705 device. Pixel (0,0) is the first pixel to be read out in using default settings for the invert/revert, windowing, and line repeat features. This mode of operation is chosen for a normal 'inverting optic'. Given this type of optic, a 'normal' raster scan image will be presented by placing the bottom row (row 0) at the 'bottom' of a camera system.

When two outputs are selected, the first pixel is presented at OutA, and the second pixel is presented at OutB. Alternate pixels are presented at the A and B output channels, respectively. When four outputs are selected, the first pixel is presented at OutA, the second pixel is presented at OutB, the third pixel at OutC, and the fourth at OutD.

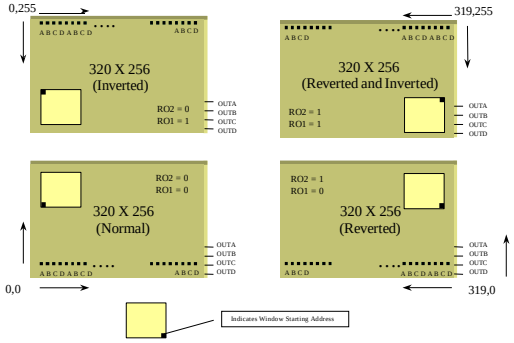


Figure 12. Four Output Mode Readout Order

Alternating in four pixel increments, pixels are presented at the A, B, C and D output channels, respectively. Figure 12. shows the assigned channels and readout order for four outputs and the various modes.

7.0 Physical Characteristics

The ISC9705 is built using a standard 0.6 micron CMOS process with double metal and single polysilicon layers. The die size is 11.35 x 10.65 mm as measured to the edge of the scribe lane. The die are processed on 5 inch (125mm) wafers which have a thickness of 625µm +/- 25µm. There are 72 die per wafer with a 200µm scribe lane in both the x and y direction. There are two standard sizes for the detector pad openings, 5.0µm or 8.0µm. Devices with 5.0µm detector pad openings are referred to as ISC97051 and devices with 8.0µm openings are referred to as ISC97052. A Mechanical Interface Database is delivered with the ISC9705 wafers. This database contains the detailed information required to design detector arrays for the ISC9705 readout device.

WARNING ! Electrostatic Discharge Sensitive Device
Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment. This can discharge with out detection and cause permanent damage. The ISC9705 features proprietary ESD protection circuitry, however permanent damage may occur on devices subjected to high energy electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or loss or functionality.